REMARKS

This is a response to the Final Office Action mailed July 27, 2005. The Final Office Action objected to claims 33 and 40, rejected claims 29 and 35-38 under 35 U.S.C. §112, rejected claims 15, 20, 28, 35-38, and 39-40 under 35 U.S.C. §102, and rejected claims 1-3, 5, 6, 8, 9, 11, 12, 23 and 30 under 35 U.S.C. §103(a).

Claims 1, 5, 15, 20, 35, 37, 39 and 40 have been amended. Claims 12, 21, 33, 34, 36, and 38 have been cancelled. Claims 41-46 have been newly added. Claims 1-6, 8-9, 11, 15, 20, 23, 24, 28, 29, 30, 35, 37, and 39-46 remain pending in this application.

Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Objections

The Office Action objected to claims 33 and 40 as informal due to a minor grammatical error. Applicants have amended claims 33 and 40 to correct the informalities noted in the Office Action. Withdrawal of this objection is respectfully requested.

Rejections Under 35 U.S.C. § 112

The Office Action rejected claims 29 and 35-38 under 35 U.S.C. §112, ¶2, as being indefinite. Applicants have amended claims 29 and 35-38 to correct the problems noted in the Office Action. Applicants respectfully request that this rejection be withdrawn.

Examiner Interview – Allowance of Claims 1, 5, 15, and 20

On or about October 17, 2005, Applicants, via their attorney Julio Loza, held a telephone interview with Examiner Chris Chu regarding the novelty of Applicant's claims. Examiner Chu indicated that independent claims 1, 5, 15, and 20 would be allowed if they were amended to

include all limitations noted as allowed or allowable in the Office Action of April 20, 2005. (See page 9 of Office Action 4-20-2005). In particular, Examiner Chu indicated that claims 1 and 5 would be allowed if they included limitations (i.e., "plurality of solder balls in staggered routing scheme") that were previously removed in Applicant's Response to Office Action of May 13, 2005. Similarly, Examiner Chu indicated that claims 15 and 20 would be allowed if they included the limitations (i.e., chip-scale packages having identical routing traces, matching coefficient of expansion, and the second surface of the memory die being exposed) of allowable claims 16 and 21, respectively.

Applicants hereby submit independent claims 1 and 5 as allowed in the Office Action of April 20, 2005. In particular, Applicants have added the "staggered routing scheme" to claims 1 and 5 which also claim - a substrate having a coefficient of expansion that matches a coefficient of expansion of a memory die to within six parts per million per degree Celsius or less, wherein the second surface of the memory die remains exposed.

Independent claim 15, incorporating the allowable subject matter of dependent claim 16, and independent claim 20, incorporating the novel limitations of dependent claim 21 noted as allowable in the Office Action of April 20, 2005, are also submitted.

As a result of incorporating every allowed or allowable limitation into claims 1, 5, 15, and 20, Applicants submit that these claims are allowable and respectfully request prompt allowance of this application.

Rejections Under 35 U.S.C. § 102

The Office Action rejected claims 15, 20, 28, and 35 under 35 U.S.C. §102(e) as being anticipated by Hayasaka et al. (U.S. Pat. No. 6,809,421) ("Hayasaka").

Independent claim 15 recites "a plurality of solder balls in a staggered routing scheme, wherein all chip-scale packages in the stacked configuration have identical routing traces." Independent claim 20 recites "all chip-scale packages in the stack having identical routing traces at every level of the stack, ... five sides of the memory semiconductor die are completely exposed and a sixth side of the memory semiconductor die is exposed for improved heat dissipation." Independent claim 35 recites "the first surface is partially exposed and the other five surfaces of the memory device are completely exposed for improved heat dissipation ... the substrate made from a different material than the memory device and having a coefficient of expansion that matches a coefficient of expansion of the memory device to within six parts per million per degree Celsius or less." Applicants submit that none of these limitations are found in Hayasaka or any of the cited prior art references.

As seen in Fig. 33 of Hayasaka, the chip stack includes two chips in one layer 152_2 and one chip in another layer 152_1. The different number of chips on each layer guarantees that Hayasaka has different chip-scale packages and routing traces on each layer. Thus, these are not identical chip-scale packages or routing traces as claimed.

Hayasaka also teaches the use of an adhesive 169 between one surface of the chip 151 and the substrate 152. (See Col. 26, lines 5-14) The present invention (claims 4, 20, 28, 29, 35, 45, and 46), on the other hand, uses no adhesive or filler on any surface of the semiconductor device to improve heat dissipation. Specifically, the present claimed invention maintains all six surfaces of the semiconductor device fully or partially exposed. Thus, Hayasaka fails to meet this limitation.

Additionally, Hayasaka teaches that the semiconductor device and substrate are both made of silicon to match their coefficient of thermal expansion. (See Col. 26, lines 8-14). The present invention (Claims 35, 37, 39, 41, 42, 43, and 44) claims that the semiconductor device and substrate are made of different materials yet have coefficient of expansions of within six parts per million per degree Celsius or less of each other. It is important to note that because of its properties, silicon substrates are disfavored as a substrate in some implementations. The present invention addresses such issue by providing relatively close coefficients of expansion while using different materials. Thus, Hayasaka also fails to teach this limitation.

As a result of these amendments, Applicants submit that independent claims 15, 20, 28 and 35, and their dependent claims are in condition of allowance.

The Office Action also rejected claims 35-38 under 35 U.S.C. §102(b) as being anticipated by Bertin et al. (U.S. Pat. No. 5,977,640) ("Bertin").

Independent claim 37 has been amended to literally or substantively include the limitation "the first surface [of the memory device] is partially exposed and the other five surfaces of the memory device are completely exposed for improved heat dissipation". Independent claims 35 and 37 have also been amended to recite "the substrate [is] made from a different material than the memory device." Applicants submit that neither of these limitations are found in Bertin or any of the cited prior art references.

The Office Action relies on chip 30 (Figure 1) in Bertin as being the claimed "substrate". However, the common meaning of a substrate is that of a surface on which circuits can be laid-out and components attached thereto. The chip 30 is simply not a "substrate" as claimed since it has a different function than a simple substrate. Usually, chips are designed to process

information, not act as a surface for coupling other components. Even if another chip 40 can be coupled to interface points of the chip 30, it does not make this chip 30 a substrate. Additionally, as amended, the claimed substrate and memory device are made of different materials. In Bertin, the material of chips 40 and 30 is the same.

Moreover, Bertin appears to teach that the chips are encapsulated (Fig. 5, item 64; Col. 3, lines 62-65). The present claims (Claims 37 and 46), on the other hand, recite that the memory device is completely exposed on five sides and partially exposed on the sixth side. Thus, Bertin fails to teach the invention as claimed.

The Office Action rejected claims 39 and 40 under 35 U.S.C. §102(e) as being anticipated by Kasatani (U.S. Pat. No. 6,617,695) ("Kasatani").

Independent claim 39, as amended, recites "memory die ... having a first surface, the first surface of the memory die mounted facing the first surface of the substrate, wherein the first surface of the memory die remains partially exposed and the other five surfaces of the semiconductor device are completely exposed." The Office Action relies on item 17 in Kasatani as teaching the memory die with exposed surfaces as claimed. However, a close reading of Kasatani shows that item 17 is actually an integrated circuit package including package body 18. (See Col. 7, lines 10-14). Unlike the present claimed invention which claims a "memory die" (which is a circuit without packaging), Kasatani teaches a packaged circuit 17. Because of its packaging 18, the circuit is not fully exposed on five surfaces as claimed. In fact, the packaged circuit 17 is completely encapsulated, which is what the present claimed invention avoids. Thus, Kasatani fails to teach the invention as claimed.

Rejections Under 35 U.S.C. § 103

The Office Action rejected claims 1-3, 5, 6, 8, 9, 11, 12, 23, and 30 under 35 U.S.C. §103(a) as being unpatentable over Hayasaka et al. (U.S. Pat. No. 6,809,421) ("Hayasaka") in view of Nishimura et al (U.S. Pat. No. 6,781,241) ("Nishimura").

As to independent claims 1 and 5, Applicants have amended these claims to literally or substantively include the limitation "the plurality of solder balls in a staggered routing scheme." (See Figure 7, for example). Neither Hayasaka nor Nishimura teach such a staggered routing scheme.

Additionally, Hayasaka teaches the use of an adhesive 169 between one surface of the chip 151 and the substrate 152. (See Col. 26, lines 5-14) The present invention (dependent claims 4 and 45) claims "the first surface of the memory die is exposed and the other five surfaces of the memory die are completely exposed for improved heat dissipation", no adhesive or filler is used on any surface of the memory die and maintains all six surfaces of the semiconductor device fully or partially exposed. Since Hayasaka teaches using adhesive on at least one surface of the chip, it fails to meet this limitation.

Additionally, Hayasaka teaches that the semiconductor device and substrate are both made of the same material, i.e. silicon, to match their coefficient of thermal expansion. (See Col. 26, lines 8-14). The present invention (dependent claims 41 and 42) claims that the semiconductor device and substrate are made of different materials yet have coefficient of expansions of within six parts per million per degree Celsius or less of each other. Thus, Hayasaka also fails to teach this limitation.

The Office Action also rejected claims 4, 33, and 34 under 35 U.S.C. §103 (a) as being unpatentable over Hayasaka in view of Nishimura and further in view of Kelly et al. (U.S. Pat. No. 5,798,567) ("Kelly").

Regarding Kelly, Applicants note that it fails to teach that "five sides of the memory die are completely exposed and a sixth side of the memory die is exposed" since an adhesive 59 is used to fully cover one surface of the memory die 41. (See Fig. 4). Thus, Hayasaka in view of Kelly fail to teach the invention as claimed.

The Office Action also rejected claims 21, 29, and 36 under 35 U.S.C. §103 (a) as being unpatentable over Hayasaka in view of Kelly et al. (U.S. Pat. No. 5,798,567) ("Kelly").

While Applicants disagree that the cited references teach the claimed invention, this argument need not be reached since claims 21, 29, and 36 have been cancelled. For the record, because Kelly teaches the use of adhesive 59 to fully cover one surface of memory die 41, it fails to teach the limitations formerly found in claims 21, 29, and 36 (i.e., every surface of the semiconductor device or memory die being completely or partially exposed).

The Office Action also rejected claim 24 under 35 U.S.C. §103 (a) as being unpatentable over Hayasaka in view of Corisis et al. (U.S. Pat. No. 6,414,391) ("Corisis").

While Applicants disagree that the cited references teach the claimed invention, this argument need not be reached since claim 24 is dependent on allowable claim 20.

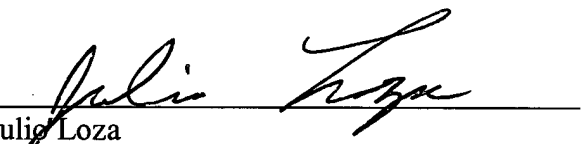
Applicants submit that as a result of the amendments made to the independent claims and the remarks distinguishing the prior art, the remaining claims are in condition for allowance.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited. Authorization is hereby given to charge our Deposit Account No. 19-2090 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,

Sheldon & Mak PC



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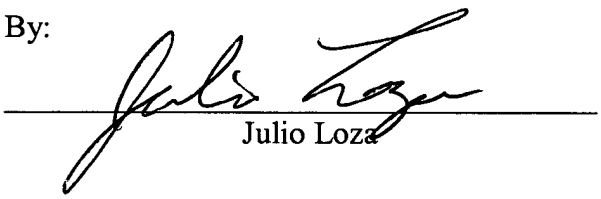

Julio Loza

Dated: October 26, 2005